AMENDMENTS TO THE CLAIMS:

The following listing of claims replaces all prior listings, and all prior versions, of claims in the application.

LISTING OF CLAIMS:

1. (Original) A memory controller comprising:

means for receiving, from a processor, a request for access to a dynamic random access memory having a data storage area divided into a plurality of banks each divided into a plurality of pages; and

memory control means for activating a page to be accessed, based on said access request from said processor, and executing, before a next request for access to a page to be accessed subsequently by said processor, precharge of said page to be accessed subsequently.

2. (Original) A memory controller comprising:

means for receiving, from a processor, a request for access to a dynamic random access memory having a data storage area divided into a plurality of banks each divided into a plurality of pages; and

memory control means for activating a page to be accessed, based on said access request from said processor, and executing, before a next request for access to a page to be accessed subsequently by said processor, precharge of a bank corresponding to said page to be accessed subsequently.

3. (Currently Amended) A memory controller for use with a processor and a dynamic random access memory, comprising:

a terminal ~~for receiving~~ adapted to receive a request for access from said processor to a dynamic random access memory having a data storage area divided into a plurality of banks each divided into a plurality of pages; and

memory control means for issuing an active command for activating a page to be accessed, based on said access request from said processor, and issuing a precharge command for executing, before a next request for access to a page to be accessed subsequently, precharge of said page to be accessed subsequently.

4. (Original) A memory controller for use with a processor and a dynamic random access memory, comprising:

a terminal for receiving a request for access from said processor to a dynamic random access memory having a data storage area divided into a plurality of banks each divided into a plurality of pages; and

memory control means for issuing an active command for activating a page to be accessed, based on said access request from said processor, and issuing a precharge command for executing, before a next request for access to a page to be accessed subsequently, precharge of a bank corresponding to said page to be accessed subsequently.

5. (Currently Amended) A memory controller comprising:

a terminal ~~for~~ adapted to receive, from a processor, a request for access to a dynamic random access memory having a data storage area divided into a plurality of banks each divided into a plurality of pages; and

a memory control unit adapted to activate a page to be accessed, based on said access request from said processor, and to execute, before a next request for access to a page to be accessed subsequently by said processor, precharge of said page to be accessed subsequently.